

MCP61PM-GM

REV:2.4

REV:A

PCB:15-V06-010010 (BLD)
BOM:81-685-V06000 for HP Nettle Model
BOM:81-685-V06001 for HP Iris Model

REV:1.0A

PCB:15-V06-011010(BLD)
PCB:15-V06-011011(GE1)
PCB:15-V06-011012(BLD OSP)
PCB:15-V06-011013(GE1 OSP)
BOM:89-386-V06100 for HP Nettle Model
BOM:89-386-V06101 for HP Iris Model
BOM:89-486-V06102 for HP Nettle Model CKD BOM

REV:1.0B

PCB:15-V06-011021(BLD OSP)
PCB:15-V06-011022(GE1 OSP)
BOM:81-685-V06111 for HP Nettle2 Model
BOM:81-685-V06112 for HP Iris V1.0B Model
BOM:81-685-V06113 for HP Iris8 Model

REV:2.0

PCB:15-V06-012000 (BLD OSP)
BOM:81-685-V06200 for HP Nettle3 cPC Model
BOM:81-685-V06201 for HP Bowie bPC Model

REV:2.1

PCB:15-V06-012100 (BLD OSP)
PCB:15-V06-012101 (GE1 OSP)
BOM:89-386-V06211 for HP Nettle3 cPC Model
BOM:89-386-V06210 for HP Bowie bPC Model

REV:2.2

PCB:15-V06- (BLD OSP)
PCB:15-V06- (GE1 OSP)
PCB:15-V06- (GBM OSP)
BOM:89-386-V06 for HP Nettle3 cPC Model

REV:2.3

ADD EUP LOT 6.0 SOLUTION
LAN CHANGE TO 8201EL


REV:2.4

FIX EUP LOT 6.0 SOLUTION

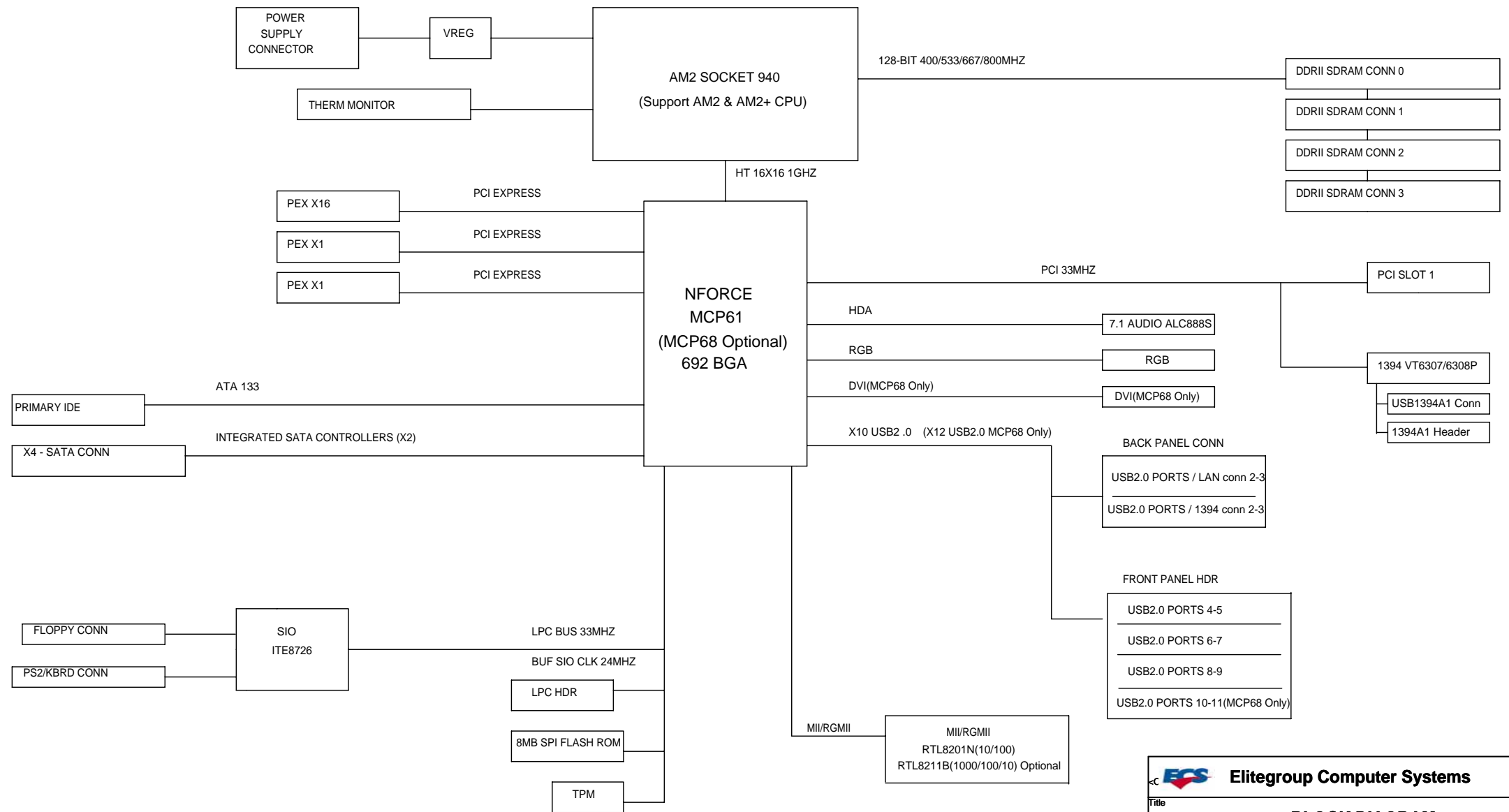
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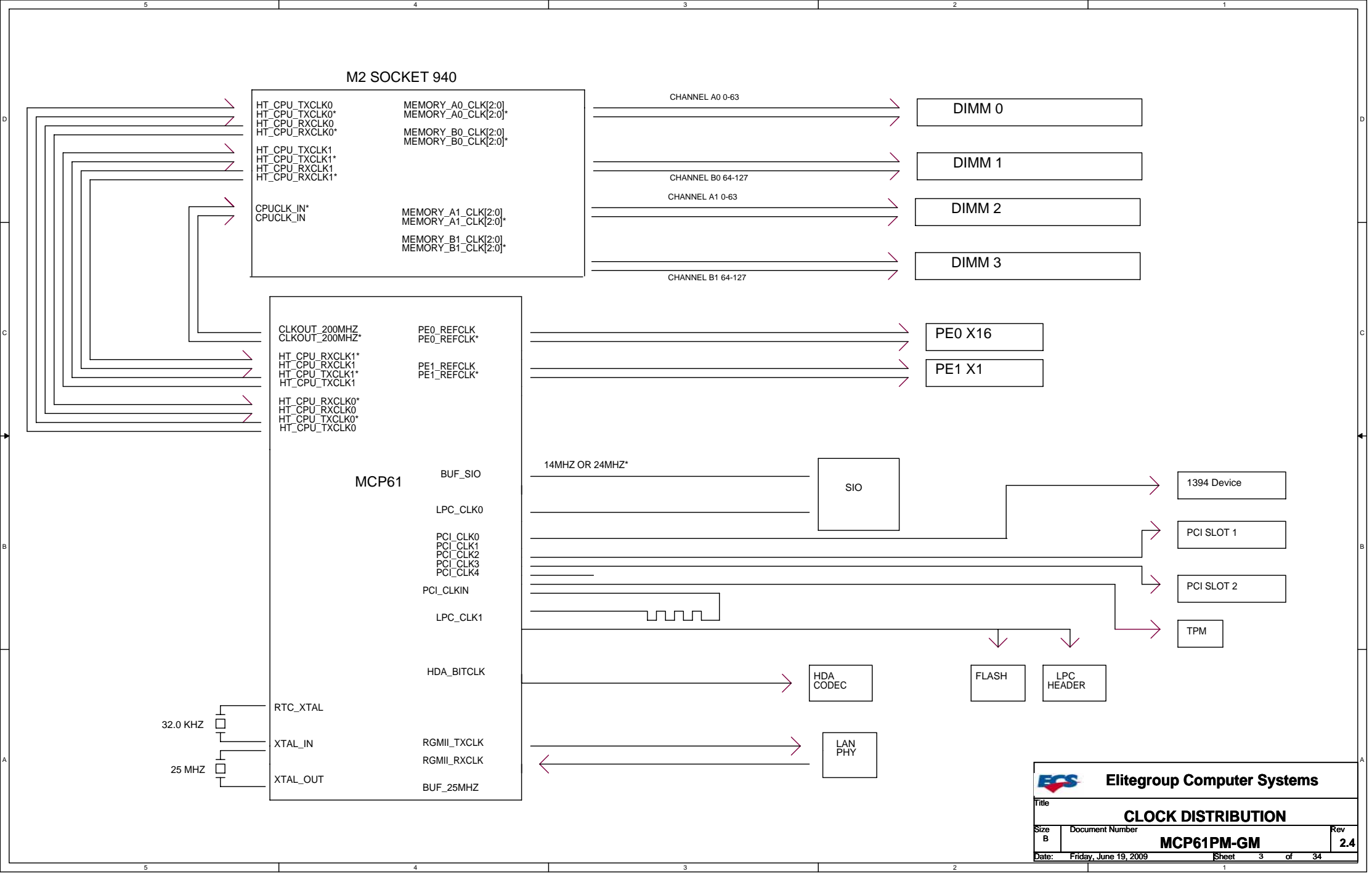
- 01-COVER PAGE
- 02-BLOCK DIAGRAM
- 03-CLOCK DISTRIBUTION
- 04-CPU M2-1 HyperTransport
- 05-CPU M2-1 DDR2
- 06-CPU M2-3 Miscellany
- 07-CPU M2-4 Power and Ground
- 08-First Logic DDR2 DIMM
- 09-Second Logic DDR2 DIMM
- 10-DDR2 Termination
- 11-MCP61 HT
- 12-MCP61 PCI-E X16
- 13-MCP61 PCI-E X1/RGMII/DAC
- 14-MCP61 PCI
- 15-MCP61 SATA/IDE
- 16-MCP61 AUDIO/USB/MISC
- 17-MCP61 PWR/GND
- 18-MCP61 DECOUPLING/SPI
- 19-VGA/DVI
- 20-1394 (VIA VT6307/VT6308P)
- 21-LAN (RTL8201EL/8211CL)
- 22-PCI-E X16 CONN
- 23-PCI1
- 24-PCI-E X1
- 25-LPC SIO-ITE8726 / FDD
- 26-PS2
- 27-USB
- 28-AUDIO ALC888S
- 29-AUDIO ALC888S(PANEL)
- 30-PWR CON/FNT PNL
- 31-CPU VCORE
- 32-DC-DC
- 33-EU6 SOLUTION
- 34-ATTENTION

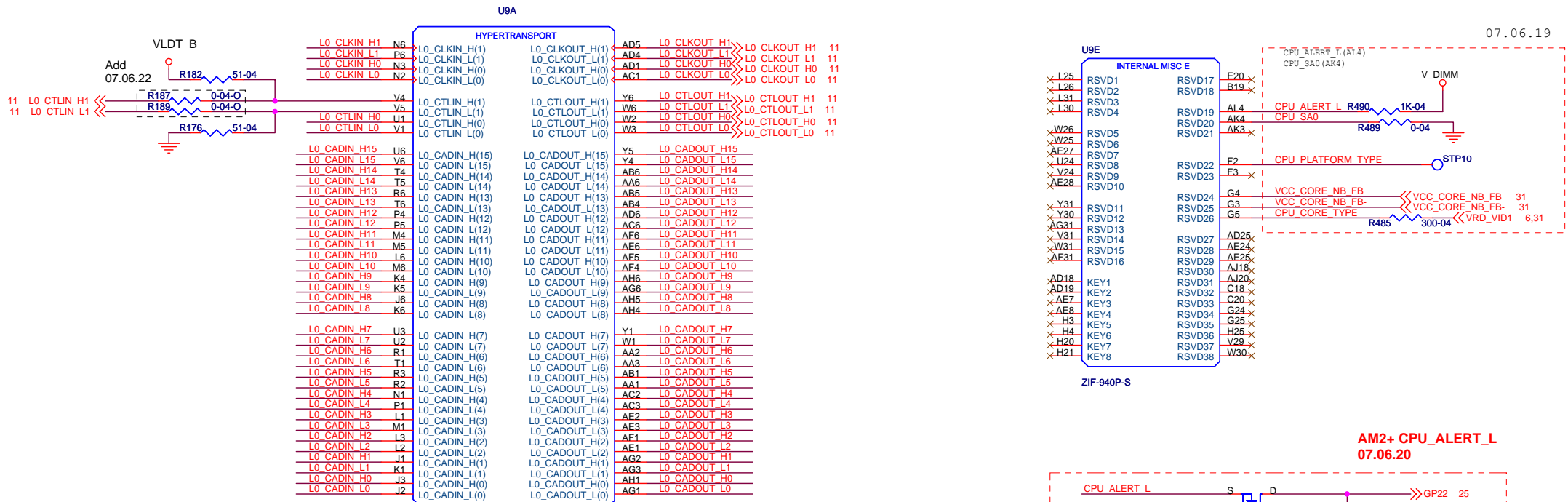
V2.4	Signature	Date
Designer		
Layout		
Check		
Approval		

 Elitegroup Computer Systems			
Title			
COVER PAGE			
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BLOCK DIAGRAM





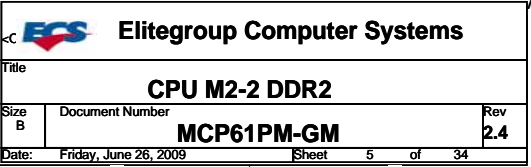


If routing to a chipset that doesn't support HyperTransport 3:

- L0_CTLIN_H(1) should be connected to VLDT_RUN using 49.9 Ohm resistor
- L0_CTLIN_L(1) should be connected to GND using 49.9 Ohm resistor

L0_CLKIN_H1 >> L0_CLKIN_H1 11
L0_CLKIN_L1 >> L0_CLKIN_L1 11
L0_CLKIN_H0 >> L0_CLKIN_H0 11
L0_CLKIN_L0 >> L0_CLKIN_L0 11
L0_CTLIN_H0 >> L0_CTLIN_H0 11
L0_CTLIN_L0 >> L0_CTLIN_L0 11

L0_CADIN_L[0..15] << L0_CADIN_L[0..15] 11
L0_CADIN_H[0..15] << L0_CADIN_H[0..15] 11
L0_CADOUT_H[0..15] << L0_CADOUT_H[0..15] 11
L0_CADOUT_L[0..15] << L0_CADOUT_L[0..15] 11



VREF25 R168 10K-04

U7A OP358-S

Q38 2N7002-S

EC25 100u-16DE

+12V

VCC3

+2.5V_VDDA

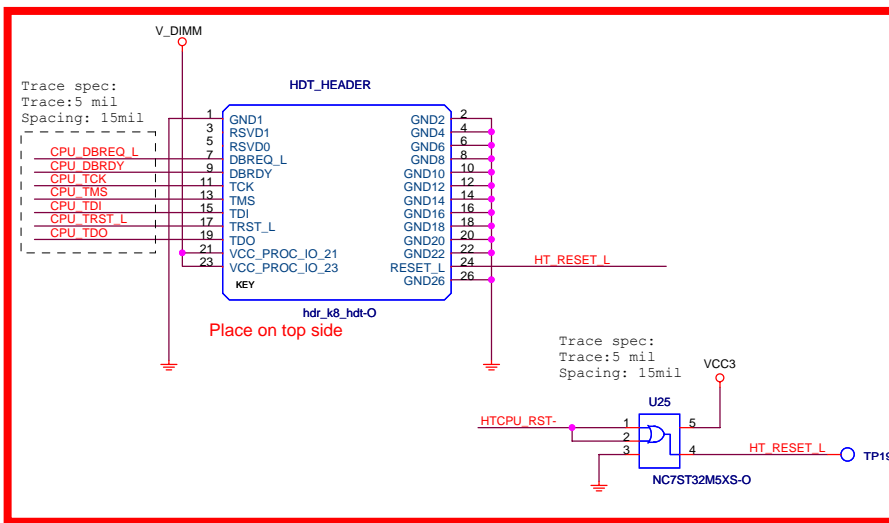
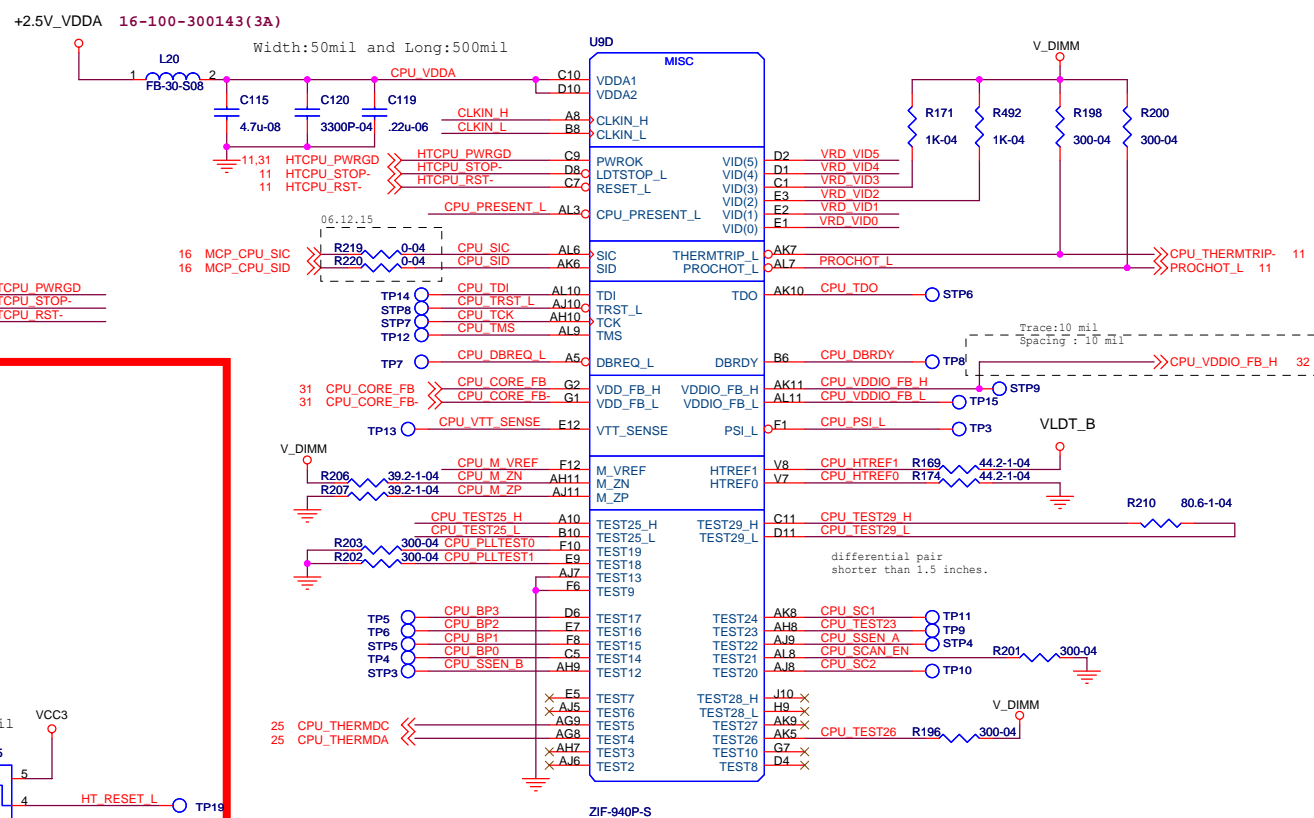
+2.5V_VDDA@105mA

V_DIMM

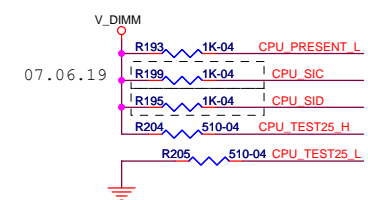
R197 300-04 HTCPU PWRGD

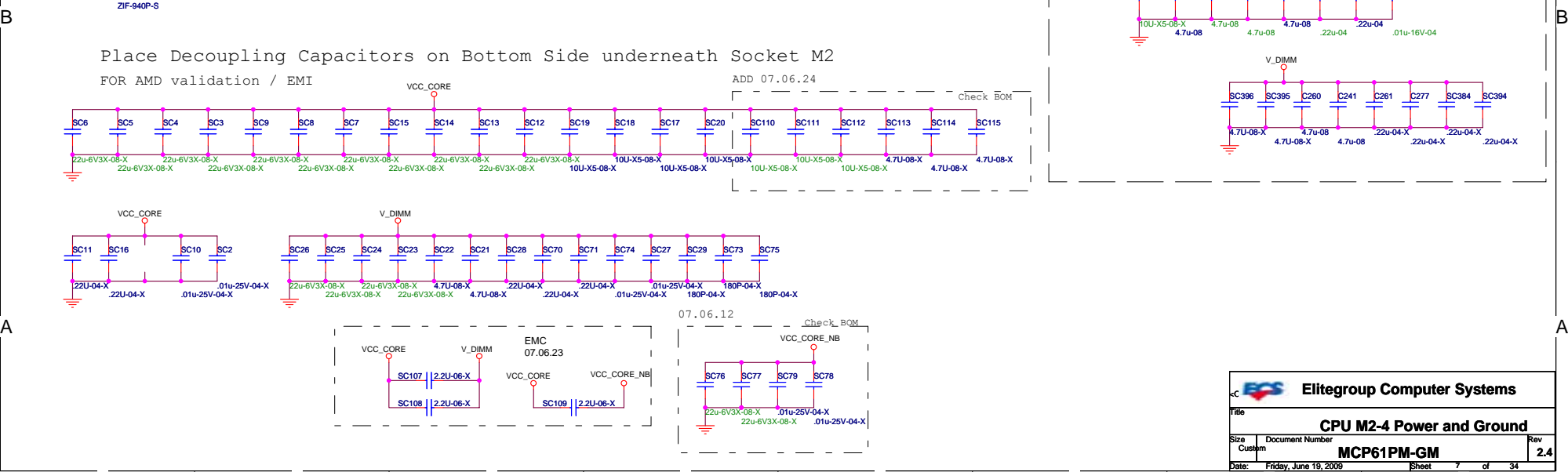
R191 300-04 HTCPU STOP

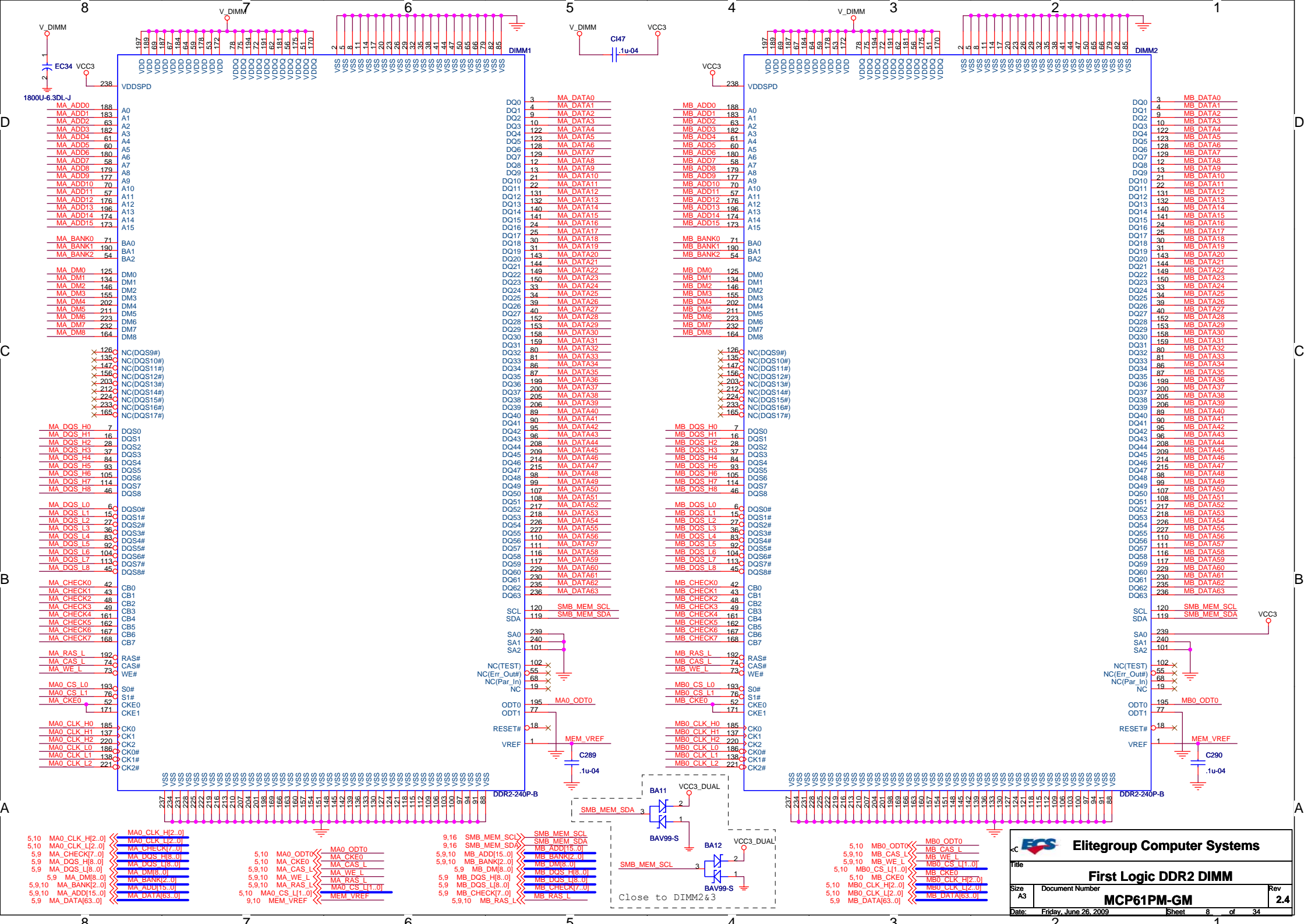
R192 300-04 HTCPU RST-

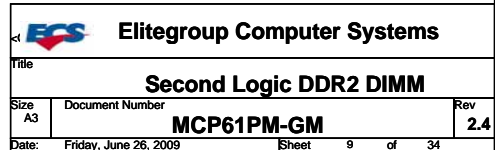
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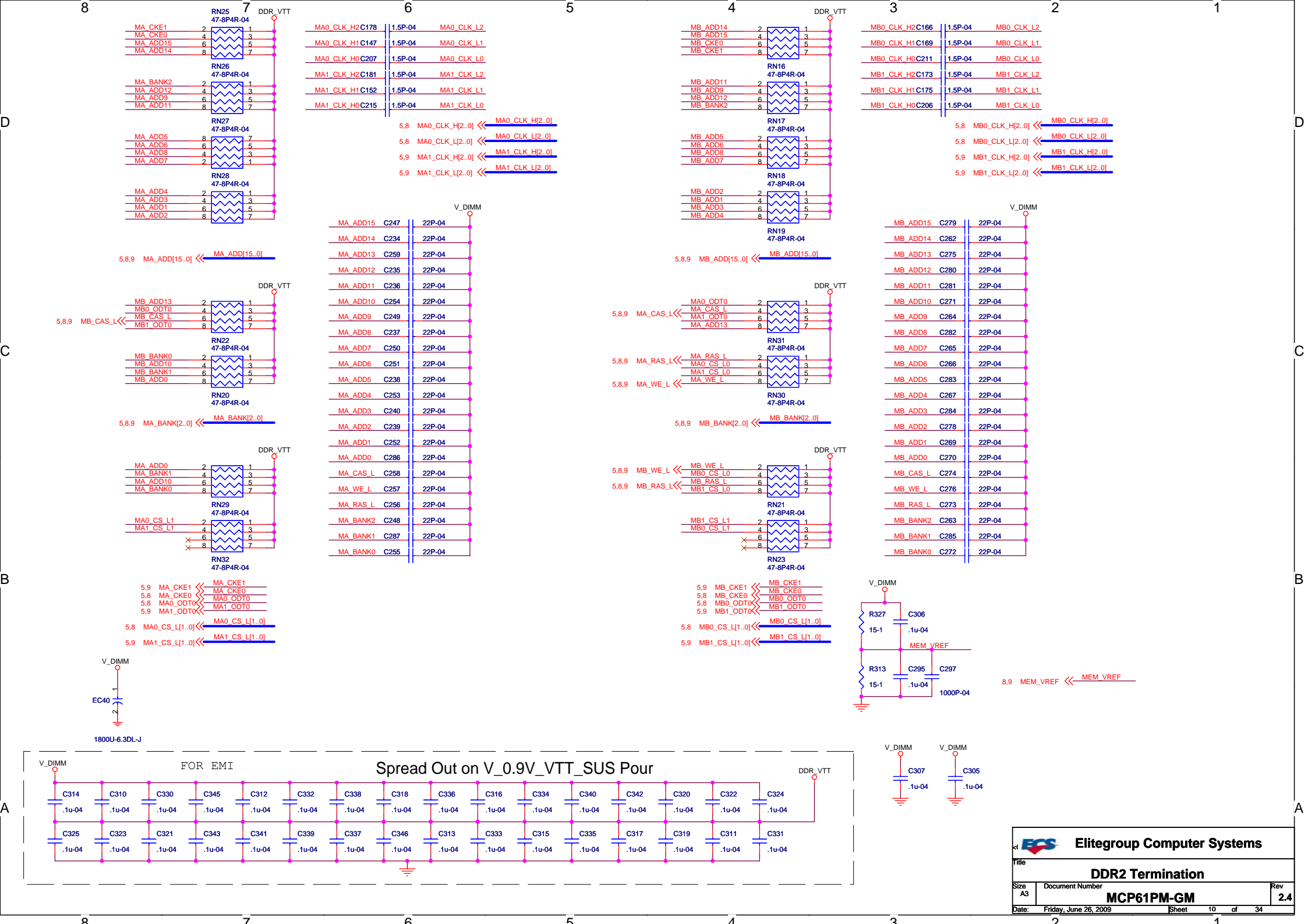
	Used	Unused
(CPU_SIC) R219	0 ohm CPU_SIC connect to MCP61	NC
(CPU_SID) R220	0 ohm CPU_SID connect to MCP61	NC
(CPU_SIC) R199	1K pull up to V_DIMM	390 ohm
(CPU_SID) R195	1K pull up to V_DIMM	NC
(CPU_SA0) R489	0 ohm pull to GND	NC
(CPU_ALERT_L) R490	1K pull up to V_DIMM	NC

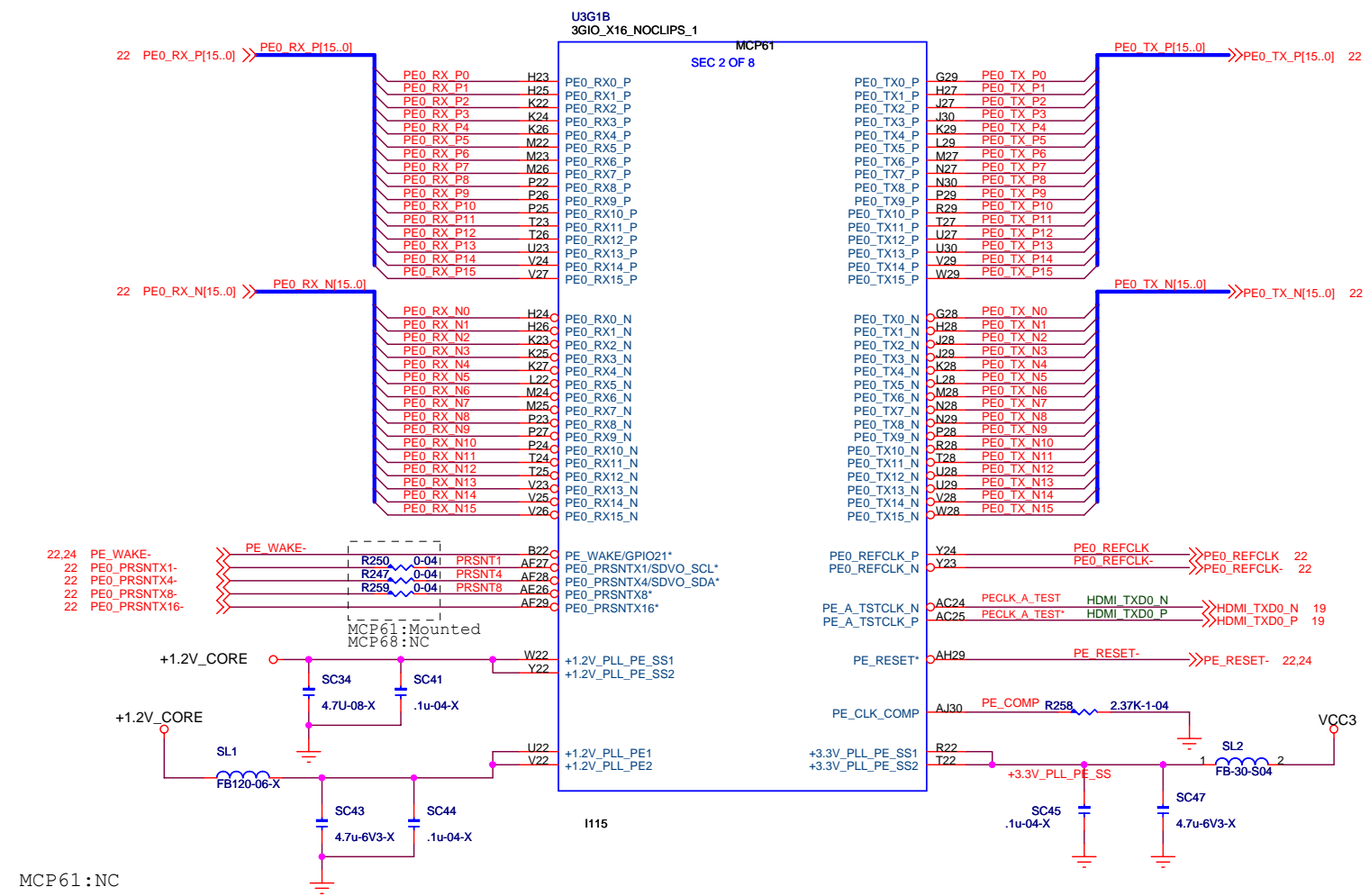




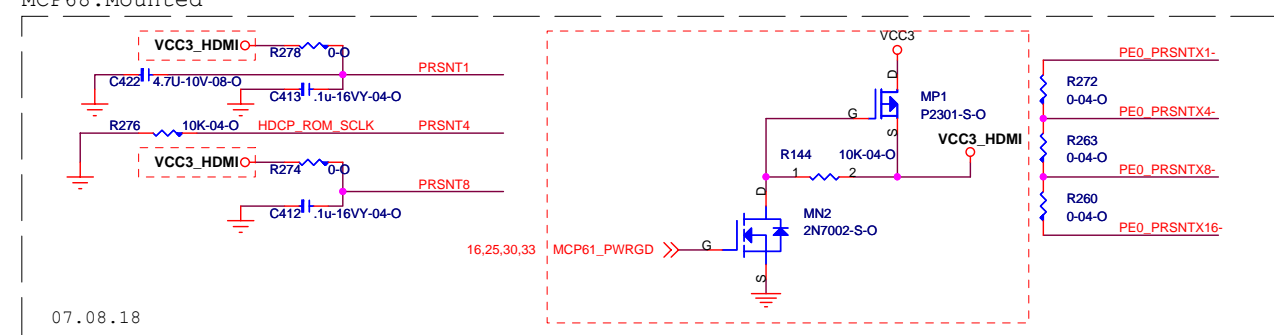


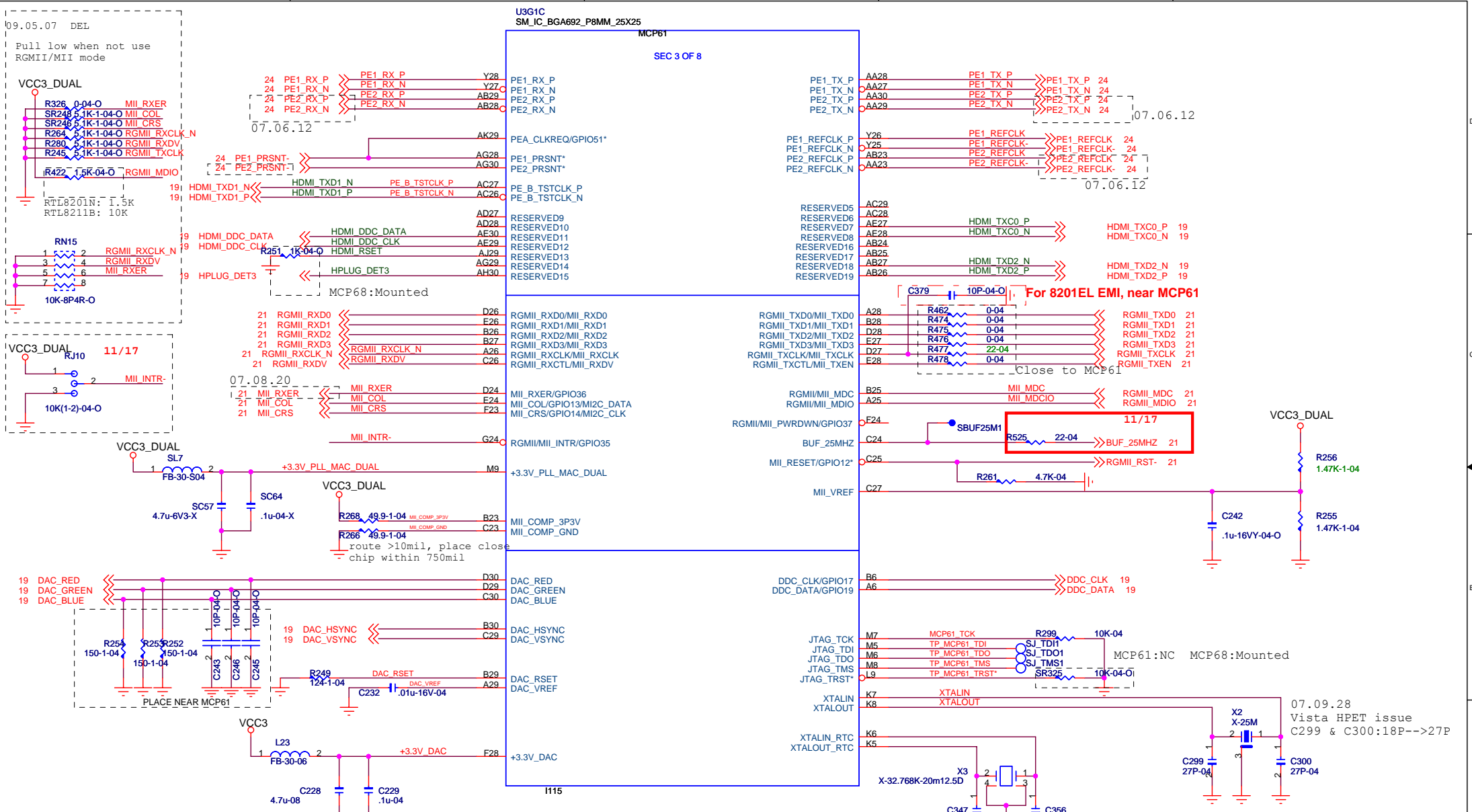






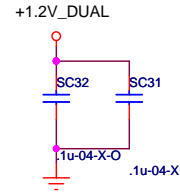
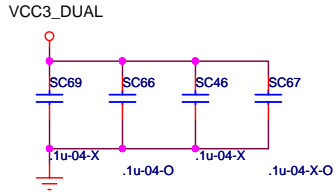
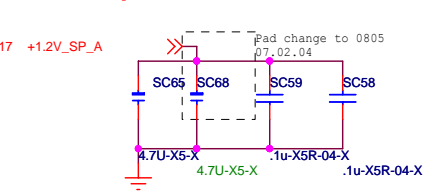
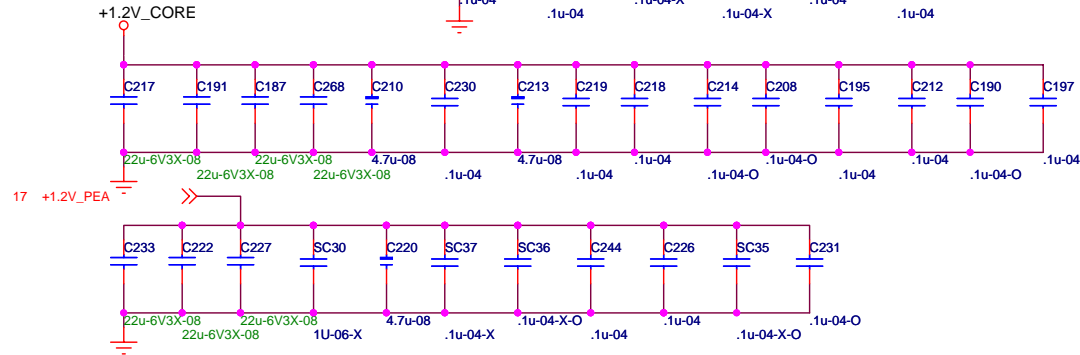
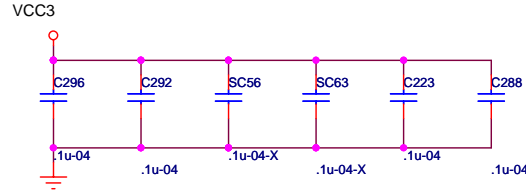
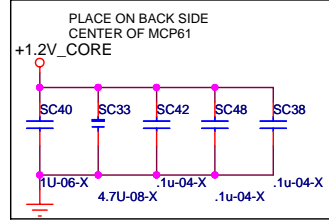
MCP61 Pin Define	MCP68 Pin Define
PRSNTX1 (AF27)	+3.3V_HDMI_PLL_HVDD
PRSNTX4 (AF28)	HDCP_ROM_SCLK
PRSNTX8 (AE26)	+3.3V_HDMI
GND (AF30)	HDCP_ROM_SDATA





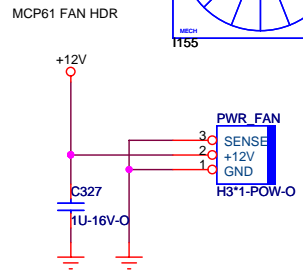
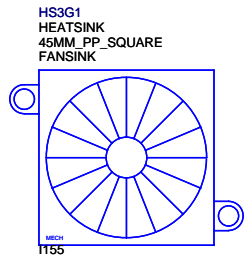


MCP61 DECOUPLING/EMI

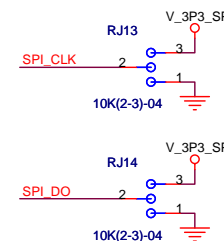
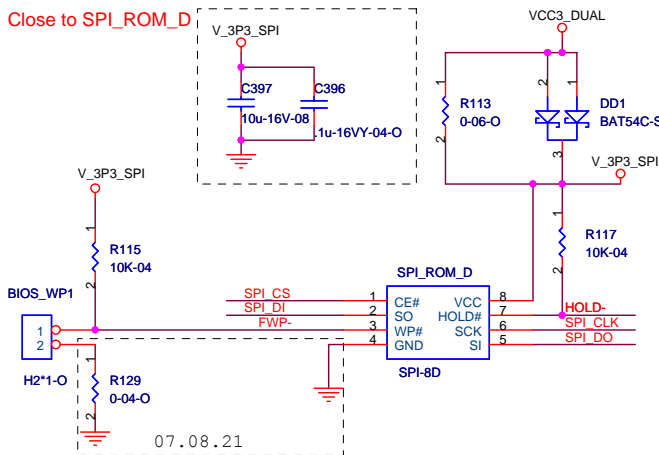


MCP61 INTERNAL PULL-UP/DWN'S

PE0_PRSNTX16*	10K PU TO 3.3V
PE0_PRSNTX8*	10K PU TO 3.3V
PE1_PRSNT*	10K PU TO 3.3V
PE2_PRSNT*	10K PU TO 3.3V
PE1_CLKREQ*	10K PU TO 3.3V
PCI_PME*/GPIO_30	8.2K PU TO 3.3V_DUAL
LPC_AD0	8.2K PU TO 3.3V
LPC_AD1	8.2K PU TO 3.3V
LPC_AD2	8.2K PU TO 3.3V
LPC_AD3	8.2K PU TO 3.3V
LPC_DRQ1/LPC_CS*	8.2K PU TO 3.3V
LPC_DRQ0*	8.2K PU TO 3.3V
LPC_SERIRQ	10K PU TO 3.3V
HDA_SDATA_IN1/GPIO_23/MGPIO_0	10K PD TO GND
HDA_SDATA_IN0/GPIO_22	10K PD TO GND
JTAG_TMS	10K PU TO 3.3V
JTAG_TRST*	10K PD TO GND
JTAG_TDI	10K PU TO 3.3V
A20GATE	10K PU TO 3.3V
PE_WAKE*	10K PU TO 3.3V_DUAL
EXT_SMI*/GPIO32	10K PU TO 3.3V_DUAL
THERM*/GPIO_59	10K PU TO 3.3V
KBRDRSTIN*/GPIO_58	10K PU TO 3.3V
R1*/GPIO_33	10K PU TO 3.3V_DUAL
SIO_PME*/GPIO_31/MGPIO_2	10K PU TO 3.3V_DUAL
PWRBBTN*	10K PU TO 3.3V_DUAL
RSTBTN*	10K PU TO 3.3V_DUAL



Close to SPI_ROM_D



MCP61 SPI CLK STRAP	MCP68 SPI CLK STRAP
SPL_DO SPI_CLK	SPI_DO SPI_CLK
00 = 500KHZ	00 = 31MHZ
01 = 1.8MHZ	01 = 42MHZ
10 = 2.5MHZ	*10 = 25MHZ
*11 = 25MHZ	11 = 1MHZ
*DEFAULT	*DEFAULT

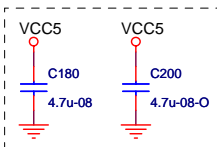
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Title: **MCP61 DECOUPLING/SPI**

Size B Document Number: **MCP61PM-GM** Rev: **2.4**

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For RGB noise
07.12.26



Close to Connector With 600 mils

V1.0 (L1,L2,L3) from FB-30-S change to INDUCTOR 68nH

VCC5

F1

FUSE-1.1A-18

2A

D5

SK24-S

VGA1:10-006-015080

DVI / D-SUB

VGA1
CONN-15P3R-FBL

VCC5

R33

2.2K-1

VCC5

R32

2.2K-1

13 DAC_RED >>> DAC_RED

13 DAC_GREEN >>> DAC_GREEN

13 DAC_BLUE >>> DAC_BLUE

L3 1 2 IND-68N

L2 1 2 IND-68N

L1 1 2 IND-68N

VGA_RED

VGA_GREEN

VGA_BLUE

VGA1
CONN-15P3R-FBL

VGA_DATA

VGA_HSYNC

VGA_VSYNC

VGA_CLK

DDC_DATA >>> DDC_DATA 13

FB120-06-B HSYNC

FB120-06-B VSYNC

DDC_CLK <<< DDC_CLK 13

R29

150-1-04

R28

150-1-04

R27

150-1-04

C11

6.8P-04

C10

6.8P-04

C9

6.8P-04

C1

6.8P-04

C2

6.8P-04

C3

6.8P-04

C38

1u-06

C5

5P-04

C4

470P-04

C6

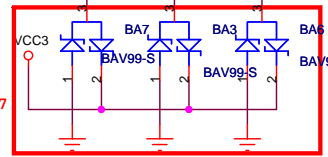
5P-04

C14

470P-04

MCP61:C5,C6-->12P

MCP68:C5,C6-->47P



11/17

VCC5

BA1

BAV99-S

BA2

BAV99-S

BA5

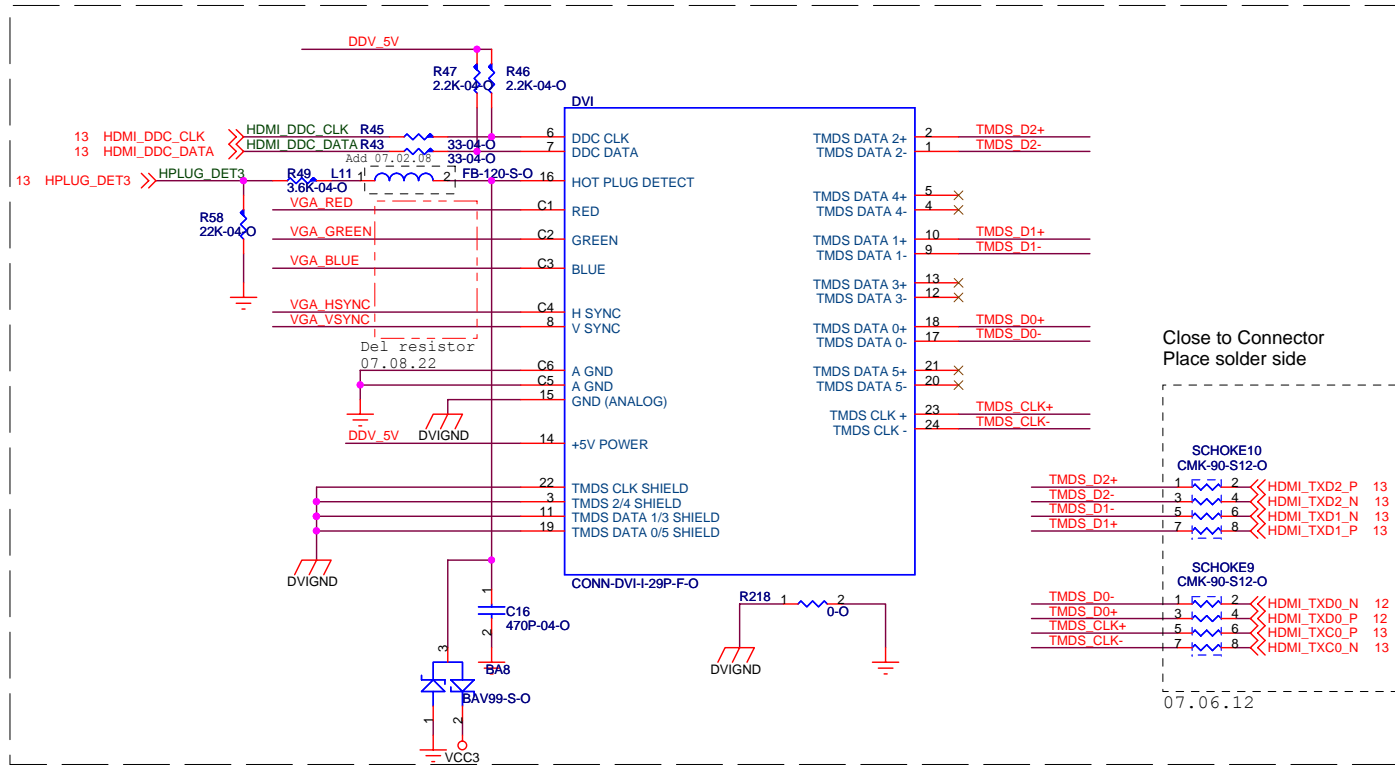
BAV99-S

BA4

BAV99-S

MCP68:Mounted

MCP61:NC



Close to Connector
Place solder side

SCHOKE10

CMK-90-S12-0

TMDS D2+

TMDS D2-

TMDS D1+

TMDS D1-

TMDS D0+

TMDS D0-

TMDS CLK+

TMDS CLK-

TMDS D2+

TMDS D2-

TMDS D1+

TMDS D1-

TMDS D0+

TMDS D0-

TMDS CLK+

TMDS CLK-

07.06.12

02-192-032130

(sub)02-192-032021

(sub)02-192-032031

13 DAC_HSYNC >>> DAC_HSYNC

74HCT32-5-S

HSYNC

VCC5

13 DAC_VSYNC >>> DAC_VSYNC

74HCT32-5-S

VSYNC

VCC5



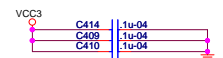
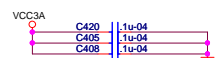
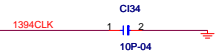
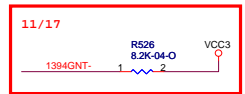
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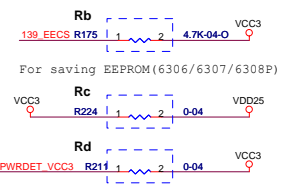
Bandgap Resistor	Ra
VT6307	6.2K-1
VT6308P	6.2K-1

BJT_SEL Internal MOS turn on
1 Use external BJT

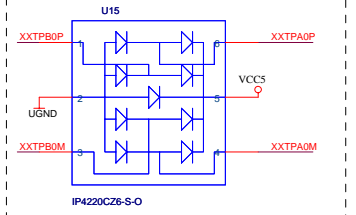
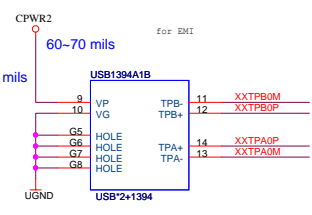
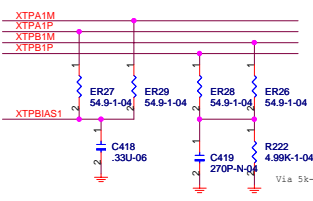
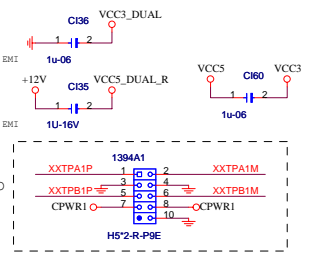
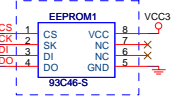
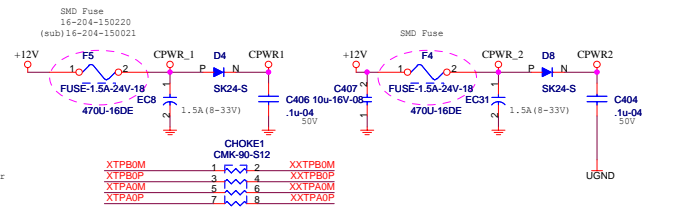
14.23 CBE-[0..3] << CBE-[0..31]
14.23 AD[0..31] << AD[0..31]



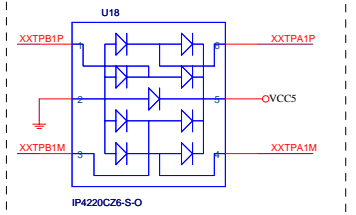
1394 CHIP (Ua)	EEPROM LESS M/B only (Rb)	EEPROM (Ub)	VDD25 Power (Rc)	PWRDET_VCC3 (Rd)
VT6307	NC(WHOL fail)	ON	ON	0 ohm
VT6308P	ON	NC	NC	4.7K



INT:Z
IDSEL:AD25
Co-layout VT6308P(PQFP)



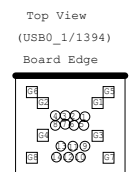
Close to USB1394A1 Connector

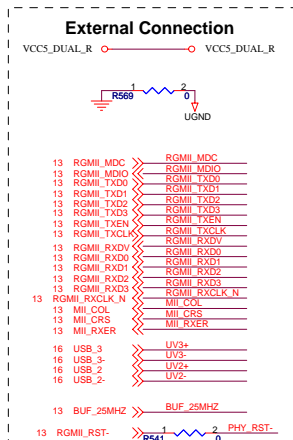


Close to 1394A1 Header

1394a:100/200/400 Mbit/sec
Impedance: Diff = 110 Ohm
Single=55 Ohm

Power Pin			
Pin	VT6307	VT6308P	
84	NC	NC	REG_FB
87	NC	NC	REG_FB
88	NC	NC	NC
35	VCC	PWRDET	
39	PVD	VCC	
49	VDD	VDD	
24	VCC	VDD	
114	VCC	VDD	
33	VCC	VDD	

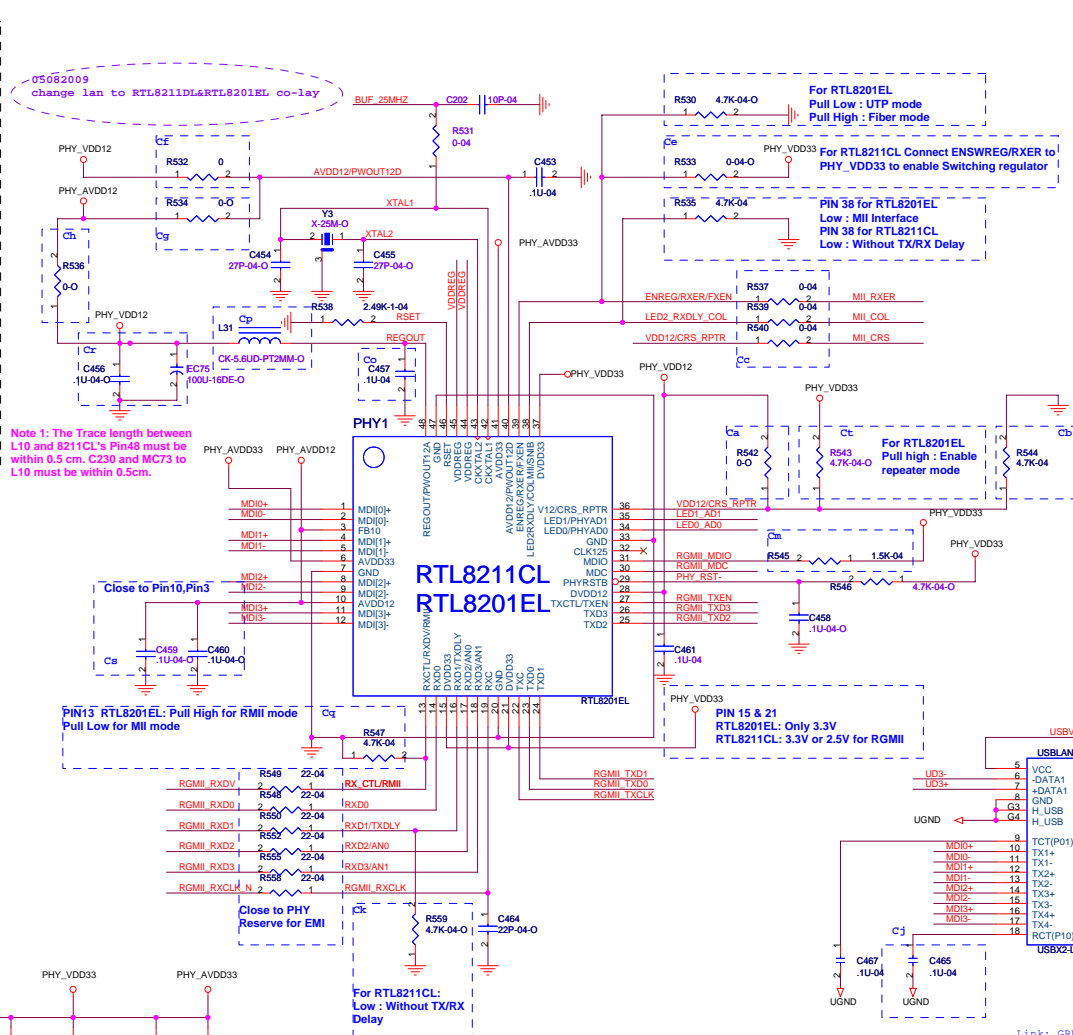


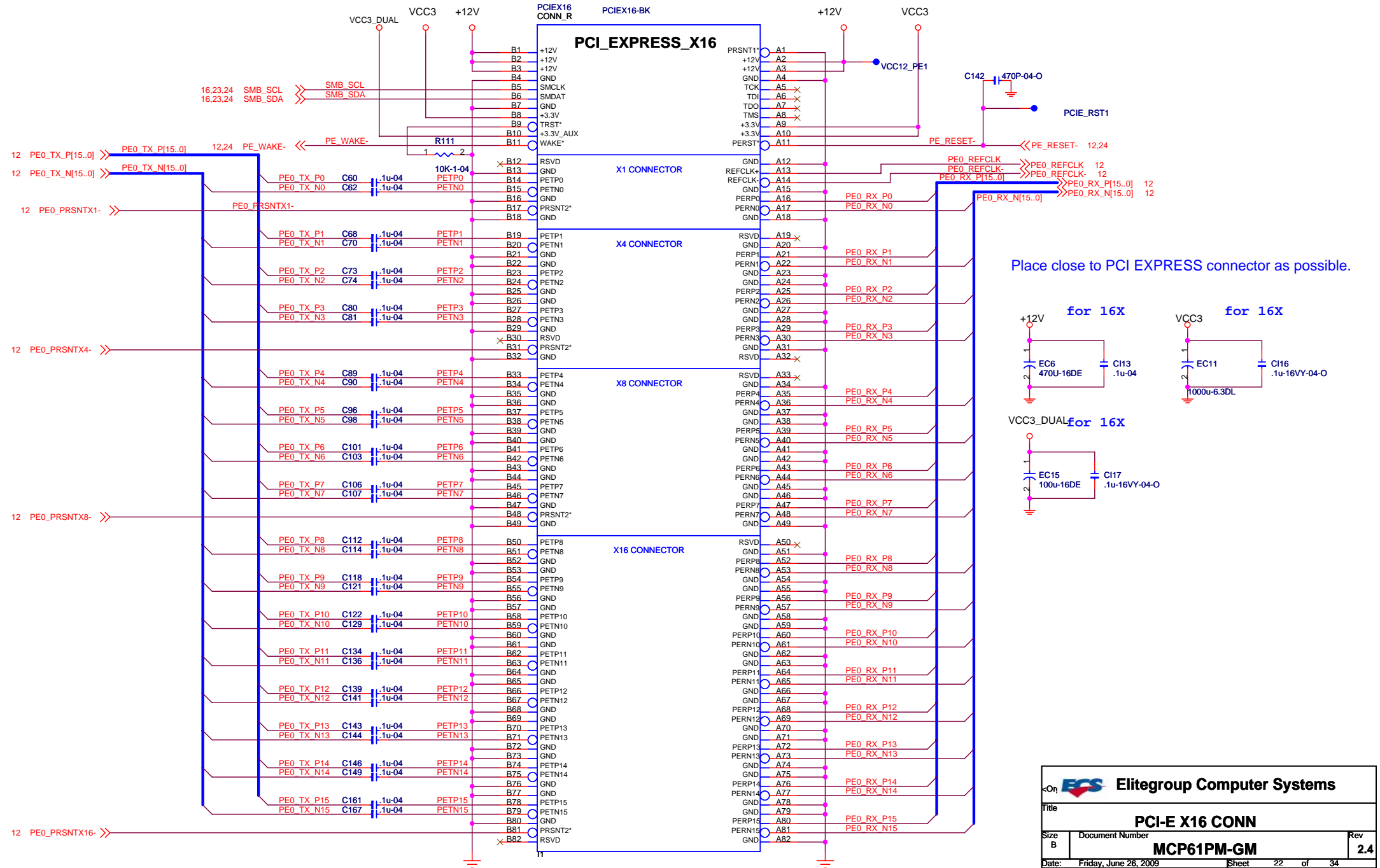


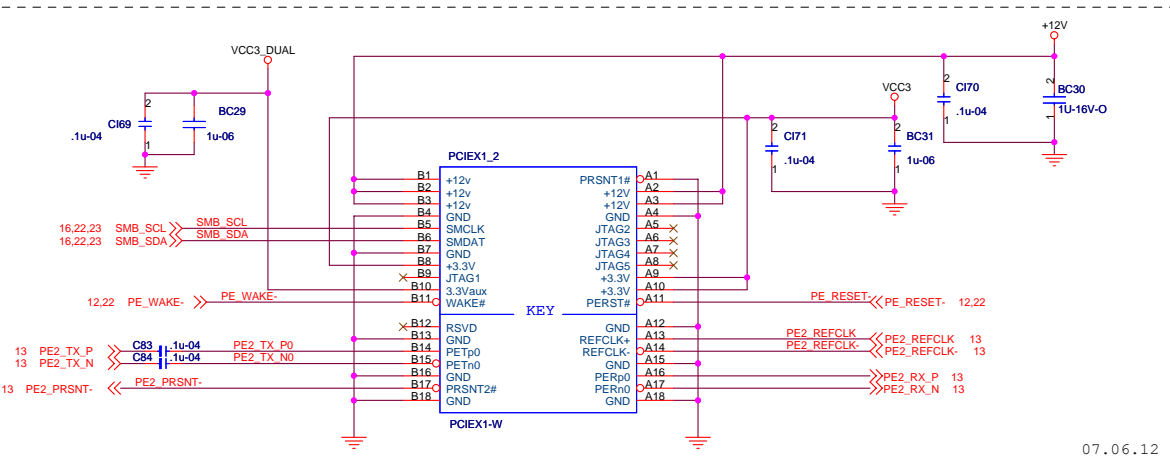
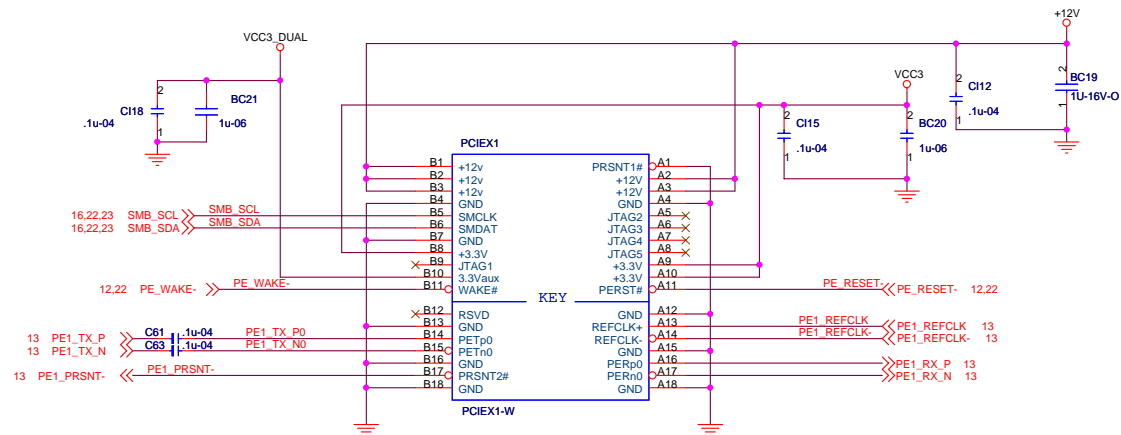
BOM Difference

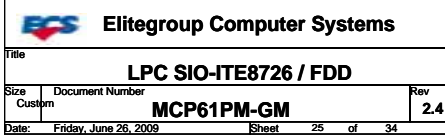
	* RTL8211CL 1000M	RTL8201EL 10/100M
Ca	0-06	X
Cb	X	4.7K-04
Cc	X	0-04
Cd	X	330-04
Ce	0-04	X
Cf	X	0-06
Cg	0-06	X
Ch	0-06	X
CI	Mount	X
CJ	.10-04	.10-04
Ck	4.7K-04	X
Cl	330-04	X
Cm	1.5K-04 (V1.7)	1.5K-04
Cn	4.7K-04	X
Co	X	.10-04
Cp	4.7uH-D	X
Cq	X	4.7K-04
Cr	.10-04 220-08	X
Cs	.10-04	X
Ct	X	X or 4.7K-04

Note 1: The Trace length between L10 and 8211CL's Pin48 must be within 0.5 cm. C230 and MC73 to L10 must be within 0.5cm.

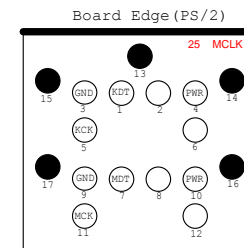
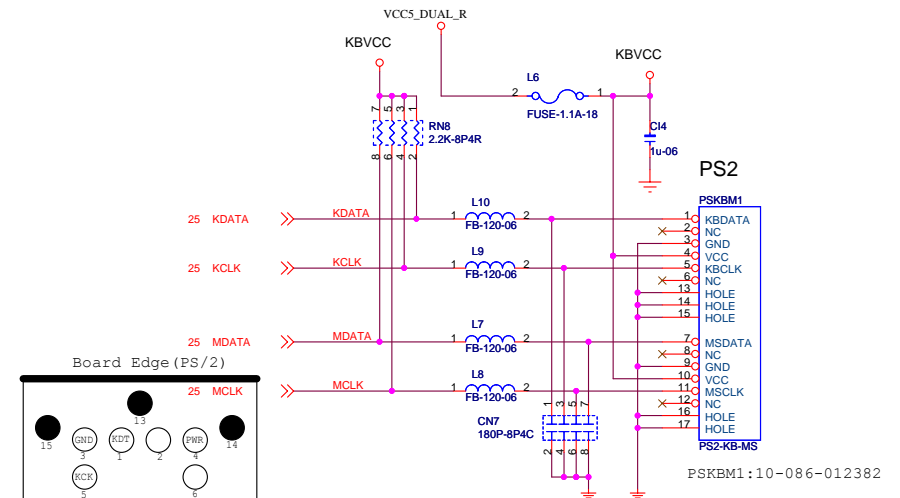
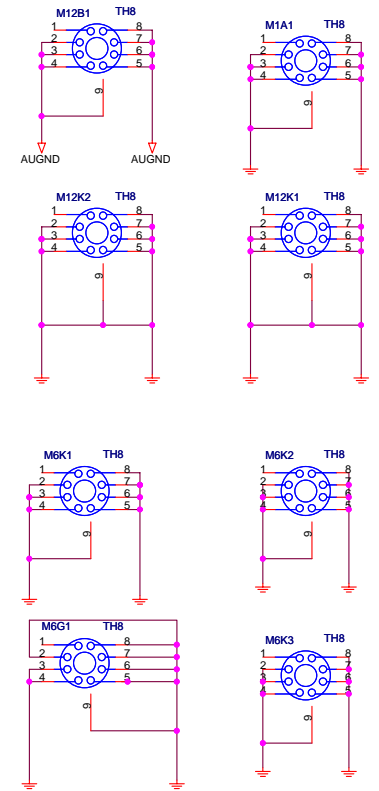
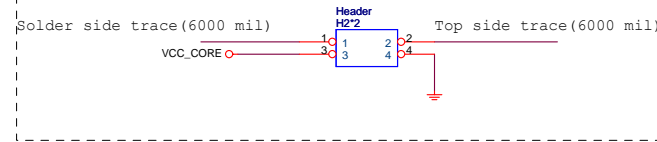


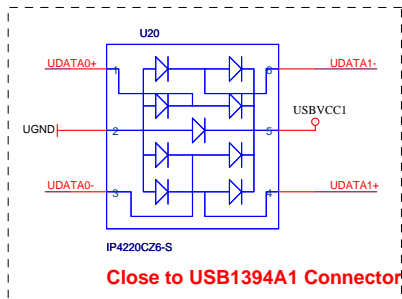
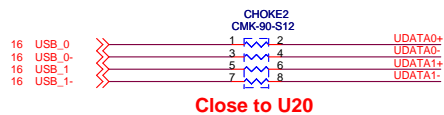




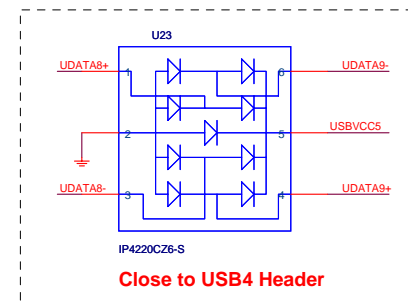
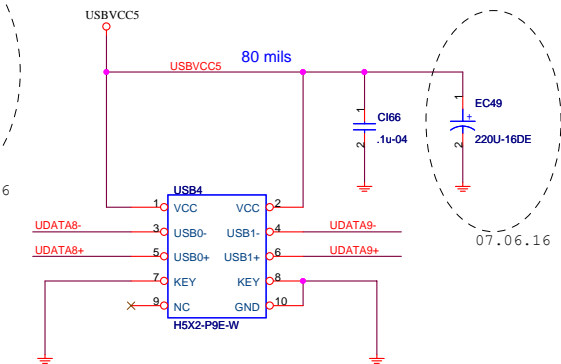
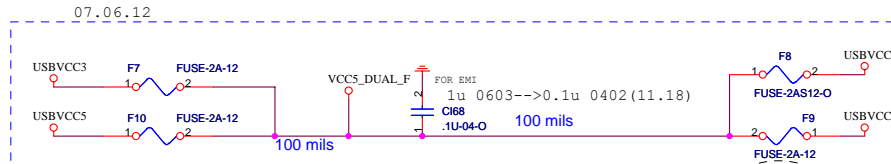
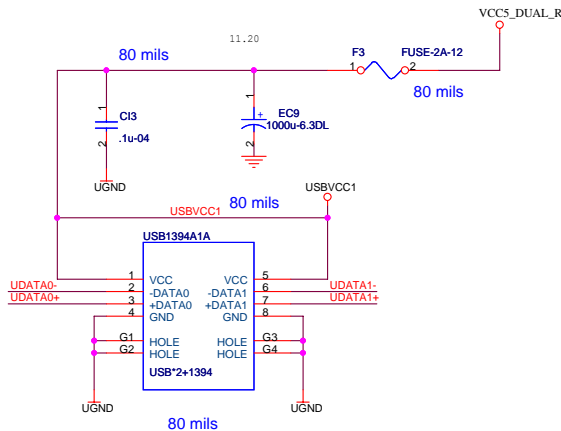


07.02.26 Impedance test

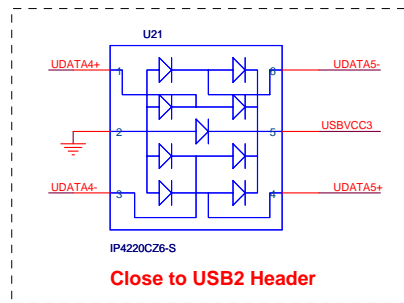
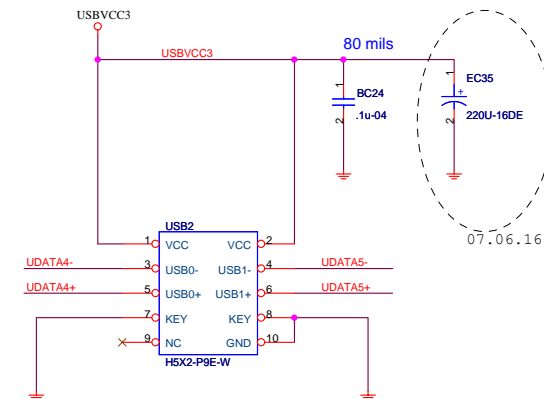




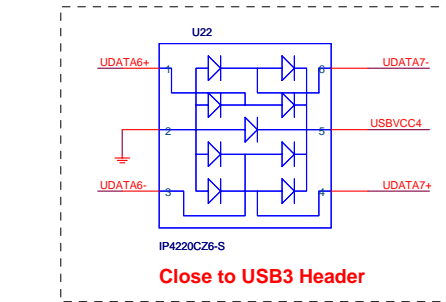
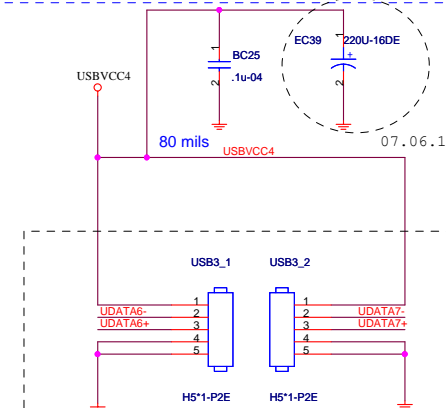
11.17 PM



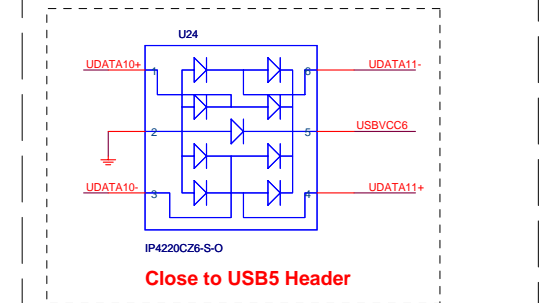
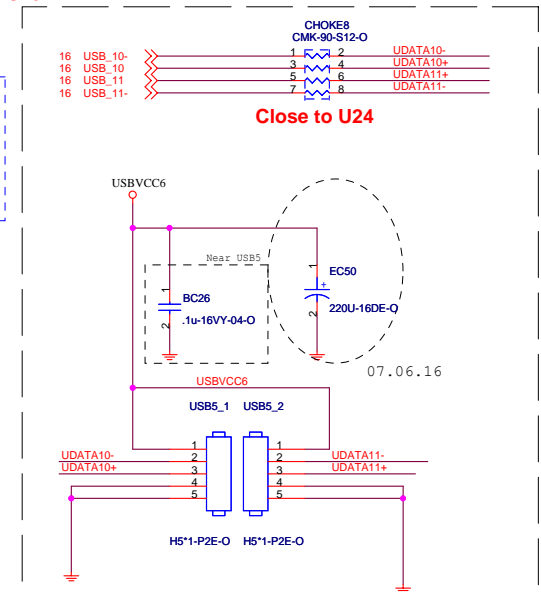
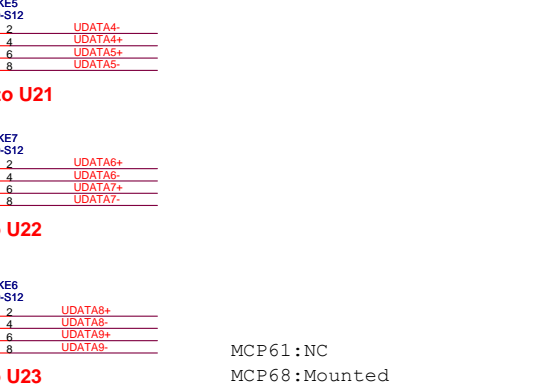
11.17 PM



11.17 PM



11.17 PM

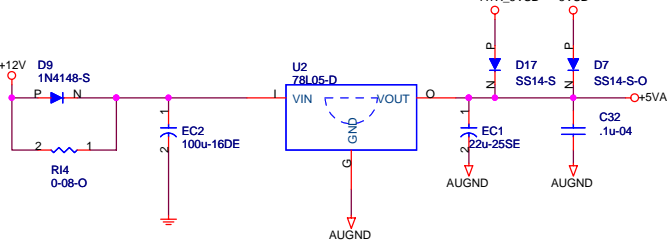


11.17 PM

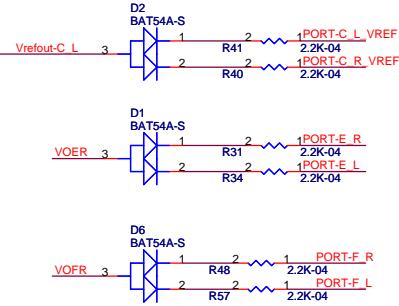
BOM Difference

Location	Nettle	Iris	Nettle2	Nettle3	bPC
Ca	ALC888	ALC888	ALC888S	ALC888S	ALC888S
Cb	V	X	V	V	X
Cc	V	X	V	V	X
Cd	V	X	V	V	X
Ce	V	X	X	X	X
Cf	X	X	V	V	V
Cg	V	X	V	V	X
Ch	V	X	V	V	X
Ci	X	X	V	V	X
Cj	X	V	X	X	V
Ck	V	X	V	V	X
Cm	V	V	V	X	X
Cn	X	X	X	X	V
Co	V	X	V	V	V
Cp	V	X	X	X	X
Cq	X	X	V	V	V
Cr	V	X	V	V	V

Improve the background noise of MIC boost

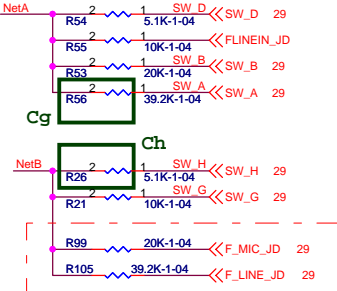


Verfourt bias for stereo microphone.

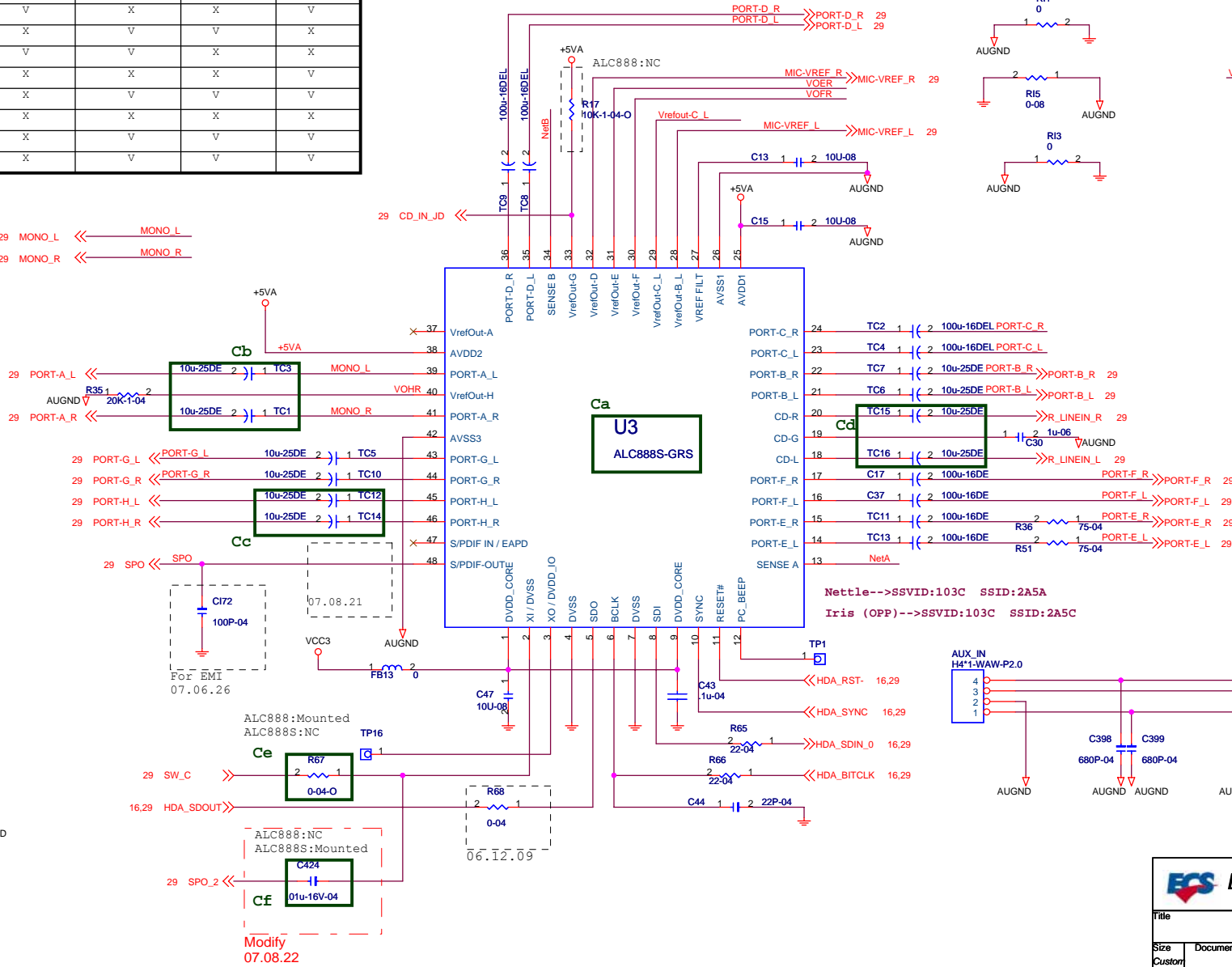


Place near Chip

Resistors Networks

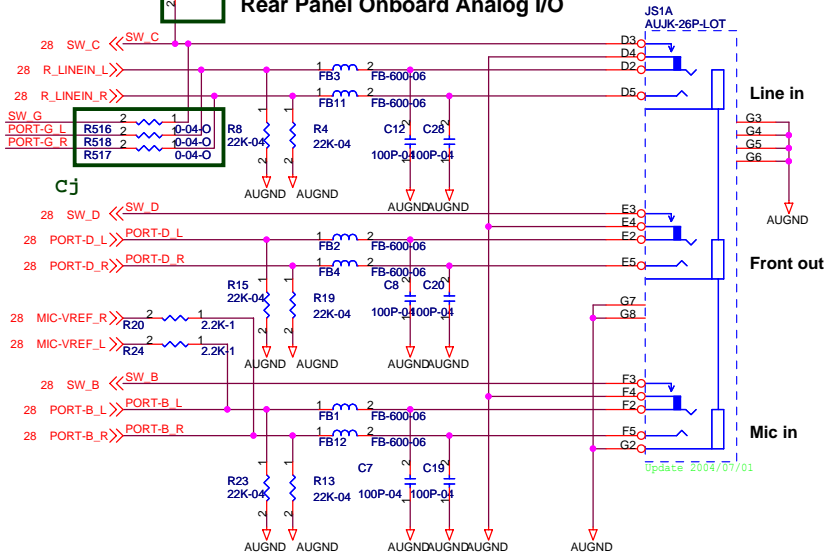


Modify 07.08.22

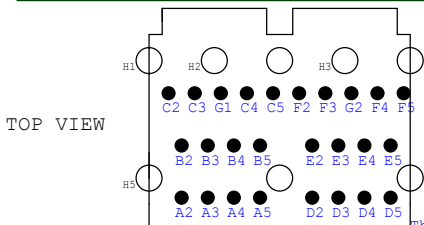
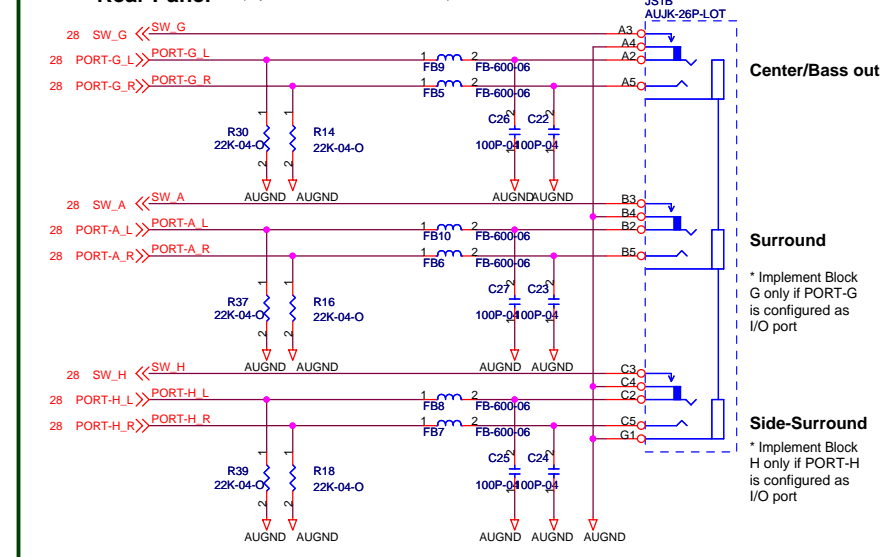


28 CD_IN_JD >> When audio chip used ALC888S(for HP),R520 must mounted.

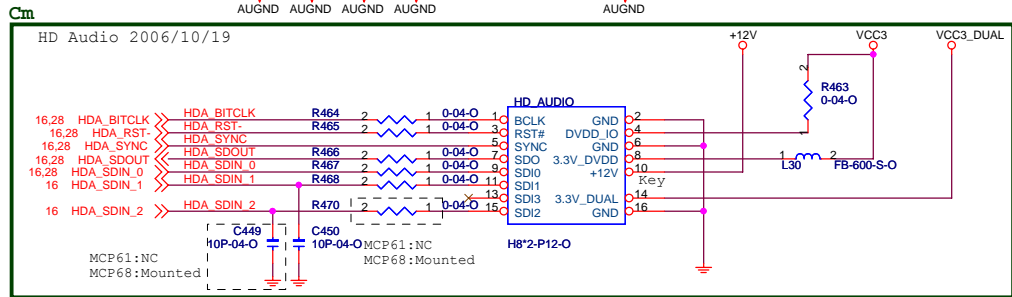
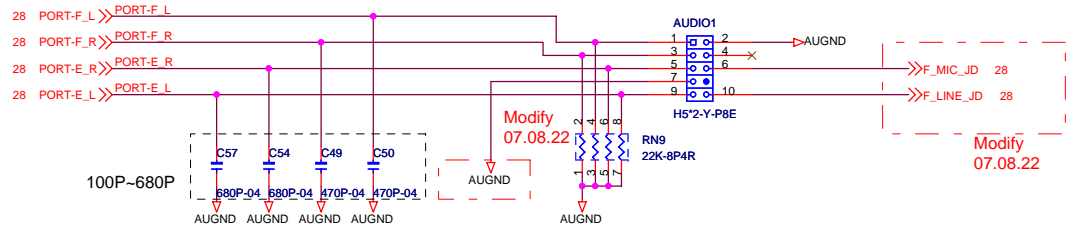
Rear Panel Onboard Analog I/O



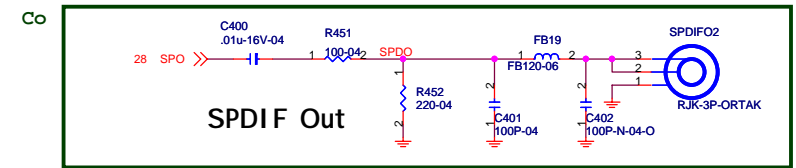
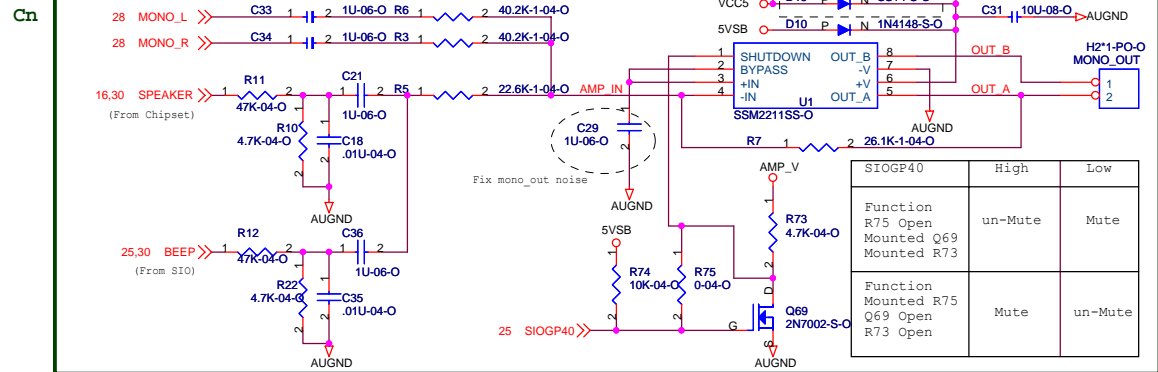
Rear Panel (Optional Rear Audio Panel)



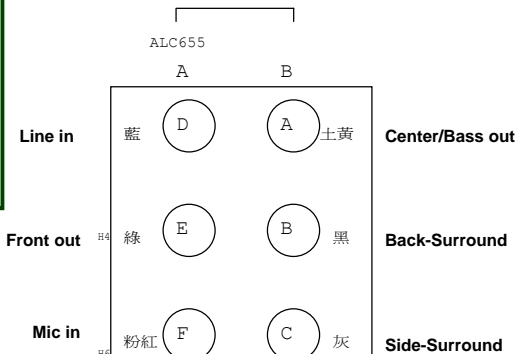
The schematic should consist with PINs define of I/O connector.



Mono Speaker
HP bPC used
07.06.19



SPDIF Out



ALC655

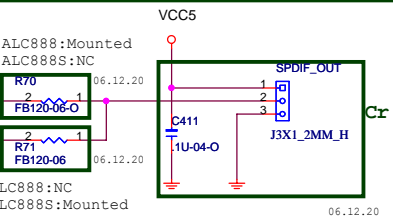
A B

藍 D A 土黃

綠 E B 黑

粉紅 F C 灰

FRONT VIEW



Elitegroup Computer Systems

AUDIO ALC888(PANEL)

MCP61PM-GM

Rev 2.4

Power for C51G Core,PCI Express,SATA

VCC5 +12V

VCC5

for MCP61@10A

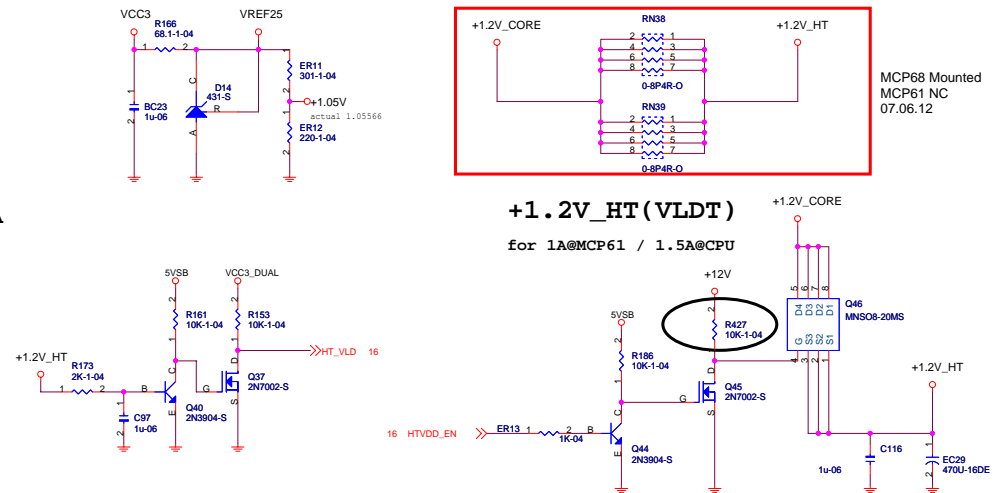
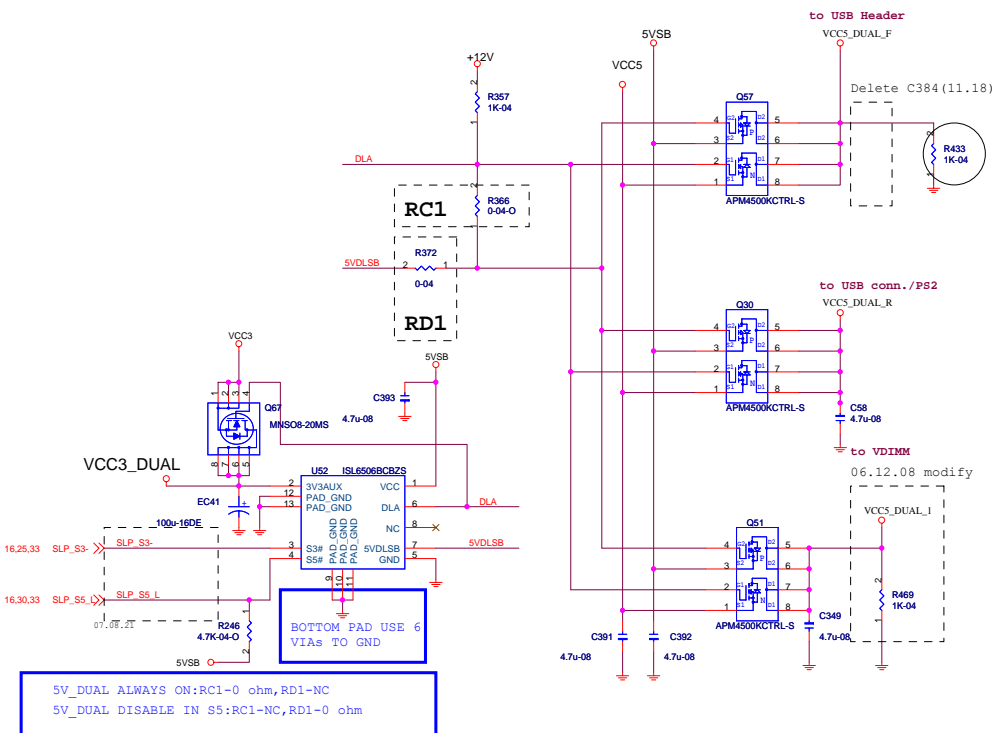
1.2V CORE

Switching Output Voltage=0.8V*(1+RT/RB)
Iocset=(40uA*Rocset+0.4V)/Rdson (low side MOSFET)

MCP68 Mounted
MCP61 NC
07.06.12

S3#	S5#	3V3AUX	VCC5_DUAL	VCC5_DUAL
1	1	3.3V	5V	S0/S1/S2 States (Active)
1	0	3.3V	5V	S3
0	1	Note		Maintains Previous State
0	0	3.3V	0V	*S4/S5(ISL6506 & 06B)
0	0	3.3V	5V	S4/S5 (ISL6506A)

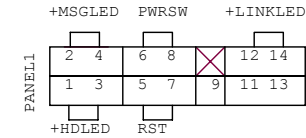
+5V_DUAL FOR USB, PS2

[illegible]

PCI_SLOT1 : REQ0, GNT0, CLK0, AD21, INT WXYX
PCI_SLOT2 : REQ1, GNT1, CLK1, AD22, INT XYZW
PCI_1394 : REQ2, GNT2, CLK2, AD25, INT Z
PCI_LAN : REQ3, GNT3, CLK3, AD24, INT Y

*

CLR CMOS	CLEAR CMOS
1-2	NORMAL
2-3	CLEAR



Modify List

Page 14,add SPI ROM
Page 19,add DVI connector
Page 20,change 1394 chip from TI TSB43A to VIA 6307/6308P
Page 21,change LAN chip from Marvell 88E8056 to Realtek RTL8201N/RTL8211B
Page 26,delete COM1,COM2,and LPT

06.11.13
ModifyAudio

06.11.14
ADDEC45,EC46

06.11.15
R267-->22K
R195-->300
R199 Pull high to V_DIMM

06.11.16
ADD R520
Modify page 13&24 PCIEX1 from PE2 to PE1,
Modify page 32,add ISL6506BCBZS ACPI control chip,and delete U15(5VSB-->VCC3_DUAL)
Modify RJ5,RJ6 10K-->8.2K
Page 18,add some SPI components

06.11.17
Page 12,modify circuit
Page 17,add R381
page 16,modify JP1,JP2
Page 19,modify BA3,BA6,BA7 to close VGA Connector

Page 20,
add R526
add U15,U18 ESD solution

page 21,add U19 ESD solution
page 27,add U20,U21,U22,U23,U24 ESD solution
Page 29,modify C449
Page 30,add R400,R429
Page 16,delete HDCP_SCL and HDCP_SDA nets,and delete R527 & R528(MCP61&68 is not used)

06.11.18
解決U3G下方放不下的問題
Page 11,SC104 0805 10u -->0603 4.7u : MCP68 design guide寫不用加,MCP68 checklist要加,MCP61不用加

Page 17, SL6 : 0603 120 ohm-->0603 30 ohm(Design guide定義)

Page 13,delete SR325

Page 32,delete C384
Page 27,delete BC30,BC27
Page 27,change BC24,BC25:0603 1u-->0402 0.1u


Page13,SR246,SR248,5.1k-->0 ohm

06.11.20
Page 20, R134&R222 4.9K-->4.99K

Page 20,U15&U18 pin5 CPWR(+12V)-->VCC5

11.21
DEL D20,R362
ADD D20(BAT54_132_1)
SWAP HD_AUDIO AUGND-->GND

2009.04.29
Page 21 Lan 由8201N改成8201EL
Page 33 add EUP LOT6.0 solution

				Elitegroup Computer Systems							
Title								ATTENTION			
Size		Document Number		MCP61PM-GM				Rev			
Custom								2.4			
Date:		Friday, June 26, 2009		Sheet		34		of 34			